Data Sheet

Anritsu envision : ensure

Signal Quality Analyzer-R

MP1900A

SQA-R

Signal Quality Analyzer-R MP1900A

Due to the explosive growth of data traffic resulting from the popularity of smartphones and mobile terminals, network interfaces are transitioning to faster 200/400 GbE standards, and PCI bus interface speeds now exceed 10G. In addition, the equipment and chipsets using these interfaces support multi-channels and multi-protocols.
The MP1900A series is a high-performance BERT with excellent expandability for supporting Physical layer evaluations of these high-speed interfaces. The all-in-one design is ideal for early stage R&D evaluations of all interfaces covering next-generation Ethernet networks to bus interconnects

Model/Order Number, Name, Option

Model/Order No.	Name
MP1900A	Signal Quality Analyzer-R
MU195020A	21G/32G bit/s SI PPG
MU195020A-001	32 Gbit/s Extension
MU195020A-010	1ch Data Output
MU195020A-020	2ch Data Output
MU195020A-011	1ch 10Tap Emphasis
MU195020A-021	2ch 10Tap Emphasis
MU195020A-030	1ch Data Delay
MU195020A-031	2ch Data Delay
MU195020A-101	32 Gbit/s Extension Retrofit
MU195020A-120	2ch Data Output Retrofit
MU195020A-111	1ch 10Tap Emphasis Retrofit
MU195020A-121	2ch 10Tap Emphasis Retrofit
MU195020A-130	1ch Data Delay Retrofit
MU195020A-131	2ch Data Delay Retrofit
MU195040A	21G/32G bit/s SI ED
MU195040A-001	32 Gbit/s Extension
MU195040A-010	1ch ED
MU195040A-020	2ch ED
MU195040A-011	1ch CTLE
MU195040A-021	2ch CTLE
MU195040A-022	Clock Recovery
MU195040A-101	32 Gbit/s Extension Retrofit
MU195040A-120	2ch ED Retrofit
MU195040A-111	1ch CTLE Retrofit
MU195040A-121	2ch CTLE Retrofit
MU195040A-122	Clock Recovery Retrofit
MU195050A	Noise Generator
MU195050A-001	White Noise
MU195050A-101	White Noise Retrofit

Signal Quality Analyzer-R MP1900A Main Frame Specifications

Functions	
Input Device, Button	Resistance film touch panel, Rotary encoder, Function button, Power button
LED	Power, Power Standby, Disk Access
LCD	12.1 inch WXGA (1280 × 800)
Ethernet	10/100/1000 Base-T RJ45 1 port (External: For remote control) 10/100/1000 Base-T RJ45 1 port (Internal: Reserved for future use)
External Display	D-Sub 15 pin 1 port HDMI Type A 1 port
USB	Front panel USB Type A 4 port Rear panel USB Type A 2 port
Module Slot	8 Slots
Functional Earth Terminal	Front panel: 2 Jacks Rear panel: 1 Terminal
OS	Windows Embedded Standard 7
Internal Storage Device	SATA 2.5-inch HDD 1 Unit (tray loading)*1
Remote Interface	GPIB, Ethernet External (automatic switchover)
Internal Reference Clock	10 MHz ± 1 ppm (Accuracy at initial shipment)
Environmental Performance	
Power Supply*2	100 V(ac) to 120 V(ac), 200 V(ac) to 240 V(ac) (automatic switching between 100 and 200 V systems), 50 Hz to 60 Hz
Power Consumption	1350 VA
Operating Temperature Range	+5° to +40°C
Dimensions and Mass	340 (W) × 222.5 (H) × 451 (D) mm (Protrusions excluded) 20 kg (excluding modules, blank panels, protective cover, power cord)
CE	
EMC	EN61326-1, EN61000-3-2
LVD	EN61010-1
RoHS	EN 50581

*1: Removing and replacing the HDD by Customer is outside the scope of warranty coverage.
*2: Operating voltage is –10% to +10% of rated voltage

Operating Bit Rate

<table>
<tr><td>Bit Rate Setting Range
(MU181000B synchronized operation)</td><td>2.400 000 Gbit/s to 21.000 000 Gbit/s, 0.000 002 Gbit/s step*1
2.400 000 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step*2
25.000 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step*2
Offset
–1000 to +1000 ppm, 1 ppm step*3</td></tr>
<tr><td>Bit Rate Setting Range
(MU181500B synchronized operation)</td><td>2.400 000 Gbit/s to 3.125 000 Gbit/s, 0.000 002 Gbit/s step
3.200 002 Gbit/s to 6.250 000 Gbit/s, 0.000 002 Gbit/s step
6.400 002 Gbit/s to 12.500 000 Gbit/s, 0.000 002 Gbit/s step
12.800 002 Gbit/s to 21.000 000 Gbit/s, 0.000 002 Gbit/s step*1
12.800 002 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step*2
25.600 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step*2
Offset
–1000 to +1000 ppm, 1 ppm step*3</td></tr>
<tr><td>Bit Rate Setting Range
(with external clock source)</td><td>When the Output Clock Rate is set to Full Rate
<table>
<tr><th>Operating Bit Rate Range</th><th>Input Clock Frequency</th><th>Relationship between Bit Rate and Clock Frequency</th></tr>
<tr><td>2.4 Gbit/s to 16.0 Gbit/s</td><td>2.4 GHz to 16.0 GHz</td><td>Operate at 1/1 clock</td></tr>
<tr><td>16.0 Gbit/s to 20.0 Gbit/s*1</td><td>8.0 GHz to 10.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 Gbit/s to 21.0 Gbit/s*1</td><td>10.0 GHz to 10.5 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>16.0 Gbit/s to 21.0 Gbit/s*2</td><td>8.0 GHz to 10.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 Gbit/s to 32.1 Gbit/s*2</td><td>10.0 GHz to 16.05 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 Gbit/s to 32.1 Gbit/s*2</td><td>6.25 GHz to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
</table>
When the Output Clock Rate is set to Half Rate
<table>
<tr><th>Operating Bit Rate Range</th><th>Input Clock Frequency</th><th>Relationship between Bit Rate and Clock Frequency</th></tr>
<tr><td>2.4 Gbit/s to 28.1 Gbit/s*1</td><td>1.2 GHz to 14.05 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>2.4 Gbit/s to 32.1 Gbit/s*2</td><td>1.2 GHz to 16.05 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 Gbit/s to 32.1 Gbit/s*2</td><td>6.25 GHz to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
</table></td></tr>
<tr><td>Bit Rate Setting Range
(MU181500B synchronized operation with external clock source)</td><td>When the Output Clock Rate is set to Full Rate
<table>
<tr><th>Operating Bit Rate Range</th><th>Input Clock Frequency</th><th>Relationship between Bit Rate and Clock Frequency</th></tr>
<tr><td>2.4 Gbit/s to 15.0 Gbit/s</td><td>2.4 GHz to 15.0 GHz</td><td>Operate at 1/1 clock</td></tr>
<tr><td>15.0 Gbit/s to 20.0 Gbit/s*1</td><td>7.5 GHz to 10.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 Gbit/s to 21.0 Gbit/s*1</td><td>10.0 GHz to 10.5 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>15.0 Gbit/s to 20.0 Gbit/s*2</td><td>7.5 GHz to 10.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 Gbit/s to 30.0 Gbit/s*2</td><td>10.0 GHz to 15.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 Gbit/s to 32.1 Gbit/s*2</td><td>6.25 GHz to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
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</table></td></tr>
</table>

*1: Not available Option x01
*2: Available Option x01
*3: Offset setting range depends on the bit rate. The range is -1000 to 0 ppm at the following bit rate.
Full Rate: 12.500000 Gbit/s, 25.000000 Gbit/s
Half Rate: 25.000000 Gbit/s

External Clock Input

Number of Input	1 (Single-end)
Input Frequency Range	1.2 GHz to 16.05 GHz
Input Amplitude	0.3 Vp-p to 1.0 Vp-p (–6.5 to +4.0 dBm)
Termination	AC, 50Ω
Connector	SMA (f)

Aux Input and Output

Aux Input	
Number of Input	1 (Single-end)
Signal Type	Error Injection, Burst, LTSSM transition
Minimum Pulse Width	1/128 of data rate
Input Level	0/–1 V (H: –0.25 V to 0.05 V, L: –1.1 V to –0.8 V) 0/–0.5 V (H: –0.05 V to 0.05 V, L: –0.55 V to –0.45 V) Select one of the above.
Termination	GND, 50Ω
Connector	SMA (f)
Aux Output	
Number of Output	2 (Differential)
Signal Type	1/n Clock (n = 4, 6, 8, 10 ... 510, 512), Pattern Sync, Burst Out2
Output Level	0/–0.6 V (H: –0.25 V to 0.05 V, L: –0.80 V to –0.45 V)
Terminator	GND, 50Ω
Connector	SMA (f)

Gating Output

Number of Output	2 (Differential)
Signal Type	Burst, Repeat
Output Level	0/–1 V (H: –0.25 V to 0.05 V, L: –1.25 V to –0.8 V)*
Terminator	GND, 50Ω
Connector	SMA (f)

*: L: Output Enable, H: Output Disable

Generated Pattern

PRBS	
Pattern Length	$2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23, 31)
Mark Ratio	1/2 (1/2INV is supported by a logical inversion.)
Zero-Substitution	
Additional Bit	0 bit, 1 bit
Pattern Length	2^n or $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23)
Start Position	Substitutes the bit coming after the maximum “0” successive bits.
Length of Consecutive Zero Bits	1 to (Pattern Length – 1) bits If the bit coming after Zero-substitution is “0”, then it is replaced with “1”.
Data	
Data Length	2 bits to 268435456 bits, 1 bit step
Mixed Pattern	
Pattern	Data
Mixed Block	To the smaller of the following values: 1 to 511 Block, 1 Block step $\mathrm{INT}\left(\frac{268435456}{\text{ROW count}} \times \text{Data length}\right)$ bits $\mathrm{INT}\left(\frac{268435456 + 2^{31}}{\text{ROW length}} \times \text{ROW count}\right)$ bits
Mixed Row Length	2048 to 268435456 + 2^{31} bits, 1024 bits step (Data + PRBS Length)
Data Length	1024 bits to 268435456 bits, 1 bit step
Number of Rows	1 to 16, 1 step
Number of Blocks	1 to 511, 1 step
PRBS Pattern Length, Mark Ratio	Same as PRBS.
PRBS Sequence	Restart, Consecutive
Scramble	Can be set per PRBS and Data for each Block (except the Data area for Block 1)

Pattern Sequence

Repeat	Continuous Pattern
Burst	
Burst Cycle	25600 bits to 2147483648 bits, 1024 bits step
Enable period	Internal: 12800 bits to 2147483392 bits, 256 bits step Ext Trigger: 12800 bits to 2147483648 bits, 256 bits step

Pre-Code

The function is available only when Pattern Sequence is Repeat.

Modulation Type	2ch Combination: DQPSK
Initial Data	Choose 0 or 1.

Error addition

Area	ALL, Specific Block (Can be selected only for Mixed.)
Internal Trigger	
Error Variation	Repeat, Single
Error Ratio	*E – n (*= 1 to 9, n = 3 to 12), Upper limit is 5E–3
External Trigger	
Control Method	External-Trigger (Rise edge trigger), External-Disable (L: Disable)

Data Output

Unless otherwise specified, these are defined with the conditions of PRBS 2^{31} – 1, Mark ratio 1/2, and Cross Point 50%.
These values are monitored using an applicable part (Coaxial Cable J1439A, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.

Number of Outputs	Option x10: 2 (Data, $\overline{\text{Data}}$) Option x20: 4 (Data1, $\overline{\text{Data}}$1, Data2, $\overline{\text{Data}}$2)
Output Amplitude	
Setting Range	0.1 Vp-p to 1.3 Vp-p, 2 mV step
Setting Error	±50 mV ±17%
Offset	
Setting Range	$-2.0 - \frac{\text{Amp.}}{2}$ to $+3.3 - \frac{\text{Amp.}}{2}$ Vth, 1 mV step
Setting Error	±65 mV ±10% of offset (Vth) ± (Eye Amp. Accuracy/2)*1
Defined Interface	NECL, SCFL, NCML, PCML, LVPECL
Cross Point	50% Fixed
Rising/Falling Time	12 ps (20 to 80%) (typ.)*1, *2, ≤15 ps (20 to 80%)*1, *2
Half Period Jitter	
Setting Range	–20 to 20, 1 step
Setting Error	±0.02 UI (typ.)*3
Jitter	Peak-to-Peak Jitter (p-p): 6 ps p-p (Measurement count 30) (typ.)*2, *4 Random Jitter (RMS): 300 fs rms (1,0 repeat pattern) (typ.)*2, *4 Random Jitter (RMS): 115 fs rms (28 Gbit/s 1,0 repeat pattern) (typ.)*2, *5 Total Jitter (Total): 6 ps (Measurement count 30) (typ.)*2, *4, *6
Waveform Distortion (0-peak)	±25 mV ±15% (typ.)*2
Data/$\overline{\text{Data}}$ Skew	±1 ps (typ.)*7
Skew Between Channels*8	±0.25 UI
Termination	AC, DC switching, 50Ω For DC: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS)
Connector	K (f)

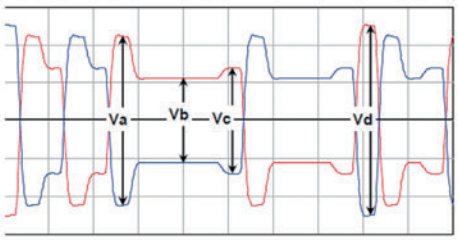
*1: Option x11 or Option x21 is installed and that Emphasis is not set.
*2: If Option x01 is not available, then this is at 21 Gbit/s.
If Option x01 is available, then this is at 32.1 Gbit/s.
Amplitude: 1.0 Vp-p
*3: When the value is set to 0.
*4: Using oscilloscope with residual jitter of less than 200 fs rms.
*5: Using oscilloscope with residual jitter of less than 70 fs rms.
*6: Defined by PRBS 2^{15} – 1, BER 10^{-12}.
*7: Cable error is not included.
*8: When Option x20 is available.

10Tap Emphasis

When Option x11 or Option x21 is added.

Emphasis Tap	10 (6 post-cursor, 3 pre-cursor)
Cursor Setting Range	–20 to +20 dB, 0.1 dB step*1
Accuracy	±1 dB (typ.)*2
Emphasis Peak Voltage Setting Range	0.1 Vp-p to 1.5 Vp-p (Single-end)
Transition Time from Idle State	≤8 ns*3

*1: Post-Cursol: $20\log_{10}(\frac{V_a}{V_b})$, Pre-Cursol: $20\log_{10}(\frac{V_c}{V_b})$



*2: Defined for the preset of 8 Gbit/s, 16 Gbit/s, and 25 Gbit/s for PCIe 3 and PCIe 4 respectively.
*3: Maximum time to transition to valid diff signaling after leaving Electrical Idle

Clock Output

These values are monitored using an applicable part (Coaxial Cable J1439A, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.

Frequency	
Full Rate	2.4 GHz to 21.0 GHz*1 2.4 GHz to 32.1 GHz*2 Operation bit rate is same as clock output frequency.
Half Rate	1.2 GHz to 10.5 GHz*1 1.2 GHz to 16.05 GHz*2 Operation bit rate is double of output clock frequency.
Number of Output	1
Amplitude	0.3 Vp-p to 1.0 Vp-p
Termination	AC, 50Ω
Connector	K (f)

*1: Option x01 not available.
*2: Option x01 available.

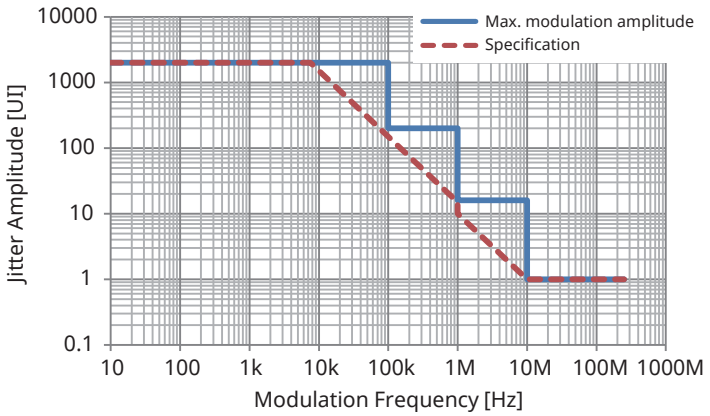
Data Delay

When Option x30 or Option x31 is available.

Phase Variable Range	–1000 mUI to +1000 mUI, 2 mUI step
Phase Setting Error	±50 mUIp-p (typ.)*
Calibration Indicator	This indicator is on when Calibration is required due to: • 1/1 Clock frequency change by ±250 kHz. • Ambient temperature change by ±5 degree.

*: When using an item with an oscilloscope residual jitter of less than 200 fs rms.

Jitter Tolerance

Jitter Tolerance Mask*	Bit rate: 16, 28.1*, 32.1 Gbit/s* Pattern: PRBS $2^{31} - 1$ SSC with a 5300 ppm amplitude and RJ of 0.3 UI can be simultaneously applied by using MU181500B. These specifications are defined assuming the following conditions: Loopback connection to the MU195040A, defined by one specific temperature in the range of 20° to 30°C. When RJ + BUJ is bigger than 0.5 UIp-p or SJ + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen.. 

Modulation Frequency [Hz]	Max. Modulation Amplitude [UIp-p]	Specification [UIp-p]
10	2,000	2,000
7,500	2,000	2,000
100,000	2,000	150
1,000,000	200	15
10,000,000	16	1
250,000,000	1	1

*: Option x01 available.

Multichannel Operation

Combination Setting*1, *2	
2ch Combination	Alternately outputs each bit in pattern as 32/64 Gbit/s band signal source to two channels.
Channel Synchronization*1	Number of channels: 2
Combination of Modules	Slot 1 to 4: 2-channel combination, channel synchronization*3
2-channel synchronization	
Output	Phase variable range –64 000 to +64 000 mUI*4 Phase variable step 2 mUI*4
Pattern	
Data	Data Length 2 × n to 268435456 × n bits, n bits step*5
Mixed	Row Length (2048 × n) to { (268435456 +2^{31}) × n }, (1024 × n) bits step*5 Data Length (1024 × n) to 268435456 × n bits, n bits step*5

*1: Option x31 is required for target channels.
*2: Combination extending over multiple slots cannot be set.
*3: When the options in the modules are the same and they are installed sequentially from slot 1,
*4: A separate value can be set for each channel. This value is common to both Channel Combination and Channel Synchronization.
*5: Common to every channel specified by Combination Setting.

Extension Function

PAM4	Supports the following by combining MU195020A with MZ1834A/B and G0375A. PAM4 signal generation • Amplitude (Single-end) 0.048 to 0.310 Vp-p (MZ1834A) • Amplitude (Single-end) 0.048 to 0.489 Vp-p (MZ1834B) • Amplitude (Single-end) 0.3 to 1.95 Vp-p (G0375A) PAM4 Emphasis signal generation (when Option x11 or Option x21 is installed) • Emphasis Peak Voltage (Single-end) 0.048 to 0.357 Vp-p (MZ1834A) • Emphasis Peak Voltage (Single-end) 0.048 to 0.564 Vp-p (MZ1834B) • Emphasis Peak Voltage (Single-end) 0.3 to 2.25 Vp-p (G0375A)

Operating Bit Rate

Operating Bit Rate	2.4 Gbit/s to 21.0 Gbit/s*1 2.4 Gbit/s to 32.1 Gbit/s*2

*1: Option x01 not available
*2: Option x01 available

System Clock

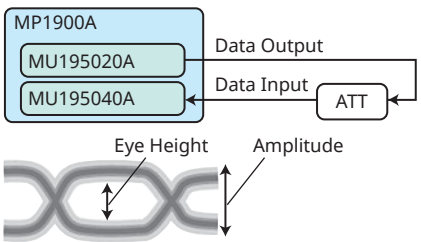
System Clock	External, Clock Recovery, Clock and Data Recovery are optional*

*: Available when Option x22 is installed. If it is not installed, only External is available.
Clock is recovered from the data input to the Data1 Input connector.

Data Input

Number of Inputs	2 (Data, $\overline{\text{Data}}$) (Differential)*1 4 (Data1, $\overline{\text{Data1}}$, Data2, $\overline{\text{Data2}}$) (Differential)*2
Amplifier	Single-end 50Ω, Differential 50Ω, Differential 100Ω can be set. At Single-end 50Ω: Data and $\overline{\text{Data}}$ can be set. At differential 50/100Ω: Tracking, Independent, Alternate can be set. When Alternate is selected: Data-$\overline{\text{Data}}$ and $\overline{\text{Data}}$-Data can be set.*3 CTLE: On/Off Switching*4
Input Signal Format	NRZ
Input Amplitude*5	0.05 Vp-p to 1.0 Vp-p
Threshold Voltage	–3.5 V to +3.3 V (1 mV step) (Can be set separately.) (Absolute value of difference between Data and $\overline{\text{Data}}$ Threshold values shall be 3 V or less.)
Input Sensitivity*5, *6, *7	Bit Rate: 21.0 Gbit/s / 28.1 Gbit/s*8 Amplitude: 19 mVp-p (typ.), ≤27 mVp-p / 22 mVp-p (typ.), ≤31 mVp-p Eye Height*9: 13 mV (typ.) / 15 mV (typ.)
Phase Margin*6, *10	Bit Rate: 21.0 Gbit/s / 25.0 Gbit/s*8 / 28.1 Gbit/s*8 / 32.1 Gbit/s*8 Phase Margin: 33 ps (typ.) / 27 ps (typ.) / 20 ps (typ.) / 18 ps (typ.)
Termination	GND, Termination Variable Selectable 50Ω
Termination Voltage	Termination Variable Setting: –2.5 V to +3.5 V, 10 mV step
Connector	K (f)
CTLE*1	
Band	Off, 8 Gbit/s to 10 Gbit/s, 16 Gbit/s to 20 Gbit/s, 25 Gbit/s to 28 Gbit/s, PCIe3, PCIe4
Peak Frequency	25 Gbit/s to 28 Gbit/s: 14 GHz (typ.) 16 Gbit/s to 20 Gbit/s, PCIe4: 8 GHz (typ.) 8 Gbit/s to 10 Gbit/s, PCIe3: 4 GHz (typ.)
Amplitude	0.05 Vp-p to 0.4 Vp-p (Input range not saturated when CTbE On)
CTLE Gain	Setting range 0 to –12 dB, 1 dB step Accuracy ±0.5 dB (typ.)

*1: Option x10
*2: Option x20
*3: Absolute value of difference between Data and $\overline{\text{Data}}$ Threshold values shall be 1.5 V or less.
*4: Option x11 or Option x21
*5: Input amplitude is a range where Auto Adjust function operates. Input sensitivity is the minimum input amplitude which becomes error-free.
*6: PRBS 31, Single-end, Mark ratio 1/2, CTLE OFF
*7: Defined by one specific temperature in the range of 20° to 30°C.
*8: Option x01
*9: Sensitivity of eye height.
Eye height is the minimum value that induces no bit error when MU195040A receives the output signal from MU195020A + ATT in the measurement system shown in the following figure (using a sampling oscilloscope of 70 GHz band or higher for measuring output amplitude)



*10: When using 0.5 Vp-p Input and External Clock.

Clock Input

Number of Inputs	1 (Single-end)
Frequency Range	1.2 GHz to 16.05 GHz
Input Level	0.3 Vp-p to 1.0 Vp-p (–6.5 to +4.0 dBm)
Termination	AC, 50Ω
Connector	SMA (f)

Aux Input, Aux Output

Aux Input	
Number of Inputs	1 (Single-end)
Input Signal	External Mask, Burst, Capture External Trigger
Minimum Pulse Width	1/128 of Data rate
Input Level	• 0/–1 V (H: –0.25 V to 0.05 V, L: –1.1 V to –0.8 V) • 0/–0.5 V (H: –0.05 V to 0.05 V, L: –0.55 V to –0.45 V) • V_{TH} 0 V (Input amplitude 0.5 Vp-p to 1.0 Vp-p)
Termination	GND, 50Ω
Connector	SMA (f)
Aux Output	
Number of Outputs	2 (Differential)
Output Signal Selection	1/n Clock (n = 4, 6, 8, 10...510, 512), Pattern Sync, Sync Gain, Error Output
Pattern Sync	PRBS, PRGM Position: 1 to (Least common multiple of Pattern Length' and 128) – 135, 8 step Pattern Length' shall be the value obtained by multiplying Pattern Length setting until it becomes 512 or more if it is 511 or less. Mixed Data Block No. setting: 1 to the Block No. specified for Mixed Data, in single steps Row No. setting: 1 to the Row No. specified for Mixed Data, in single steps
Output Level	0/–0.6 V (H: –0.25 V to 0.05 V, L: –0.80 V to –0.45 V)
Termination	GND, 50Ω
Connector	SMA (f)

Pattern Detection

PRBS	
Pattern Length	$2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23, 31)
Mark Ratio	1/2 (1/2INV is supported by a logical inversion.)
Zero-Substitution	
Additional Bit	0 bit, 1 bit
Pattern Length	2^n or $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23)
Start Position	Substitutes the bit coming after the maximum "0" successive bits.
Successive-zeros Bit Length	1 to (Pattern Length – 1) bits If the bit coming after Zero-substitution is "0," then it is replaced with "1."
Data	
Pattern Length	2 bits to 268435456 bits, 1 bit step
Mixed Pattern	
Pattern	Data
Mixed Block	To the smaller of the following values: 1 to 511 Block, 1 Block step $\mathrm{INT}\left(\frac{268435456}{\text{ROW count}} \times \text{Data length}\right)$ bits $\mathrm{INT}\left(\frac{268435456 + 2^{31}}{\text{ROW length}} \times \text{ROW count}\right)$ bits
Mixed Row Length	2048 to 268435456 + 2^{31} bits, 1024 bits step (Data + PRBS Length)
Pattern Length	1024 bits to 268435456 bits, 1 bit step
Number of Rows	1 to 16, 1 step
Number of Blocks	1 to 511, 1 step
PRBS Steps/Mark Ratio	Same as PRBS.
PRBS Sequence	Restart, Consecutive
Descramble	Can be set per PRBS and Data for each Block (except the Data area for Block 1).

Pattern Sequence

Sequence	Repeat, Burst
Repeat	Continuous Pattern
Burst	
Delay	Internal: 0 to 2147483640 bits, 8 bits step Ext Trigger, Enable: 0 to 2147483520 bits, 8 bits step Adjust Method: Auto, Manual
Enable Period	Internal: 12800 bits to 2147482624 bits, 256 bits step Ext Trigger: 12800 bits to 2147483392 bits, 256 bits step
Burst Cycle	25600 bits to 2147483648 bits, 1024 bits step

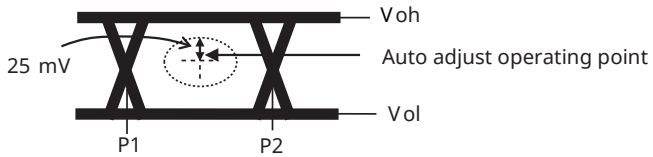
Measurement

Measurement Types	Error Rate Error Count Error Interval %Error Free Interval Frequency Frequency measurement accuracy Clock Count Sync Loss Interval Clock Loss Interval
Error Detection Mode	• Total, Insertion, Omission • Transition, Non Transition

Error Analysis

Block Window	Excludes the specified data pattern bit from the measurement target according to the settings. (Mask measurement function) Invalid when “Mixed” is selected for Test Pattern.
Bit Window	Excludes any channels among internal 32 channels from the measurement target.
Capture Function	
Automatic Measurement Function	Eye margin*1, Bathtub*1, Eye Contour*1, PAM4 BER measurement Auto Adjust*2,*3,*4, Auto Search*2, Auto Search PAM mode*5

*1: Unavailable when the system clock is set to Clock and Data Recovery.
*2: The input pattern must be an NRZ PRBS pattern with a mark ratio of 1/2.
*3: The Auto Adjust function obtains a point in the vicinity of the following as an optimum point:
• (Voh + Vol) / 2 in voltage direction
• (P1 + P2) / 2 in phase direction
The Auto Adjust function works properly when there are no mask-hits which are observed by the oscilloscope vertically within ±25 mV area from the Auto Adjust operating point.



*4: If eye diagram of input signal is not symmetry, the Auto Adjust may not adjust input signals to the optimum value.
The Auto Search Fine is recommended to measure asymmetric input signals.

Variable Clock Delay

Phase Variable Range	–1000 mUI to +1000 mUI, 2 mUI step
Phase Setting Error	±50 mUIp-p (typ.)*
Calibration Indicator	This indicator is on when Calibration is required due to: • Change in 1/1Clock frequency by ±250 kHz. • Change in the ambient temperature by ±5°C.

*: Using oscilloscope with residual jitter of less than 200 fs rms

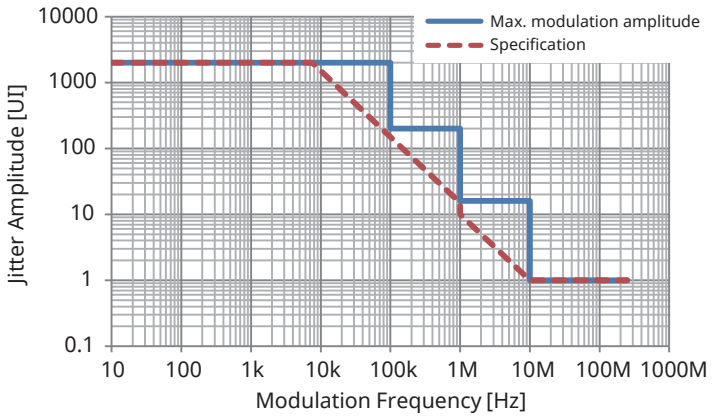
Clock Recovery

<table>
<tr><td>Clock Source Options</td><td>Clock Recovery, Clock and Data Recovery Clock*1</td></tr>
<tr><td>Operating Bit Rate</td><td>2.4 Gbit/s to 21.0 Gbit/s*2
2.4 Gbit/s to 32.1 Gbit/s*3</td></tr>
<tr><td>Setting Range</td><td>2.400000 Gbit/s to 21.000000 Gbit/s, 0.000001 Gbit/s step*2
2.400000 Gbit/s to 32.100000 Gbit/s, 0.000001 Gbit/s step*3</td></tr>
<tr><td>Maximum Number of Consecutive Zeros*4</td><td>72 bit (Zero Substitution 2^{15})</td></tr>
<tr><td>Lock Range*4</td><td>±200 ppm</td></tr>
<tr><td>Target Loop Band</td><td>Available options are $\frac{\text{Bit rate}}{1667}$ MHz, $\frac{\text{Bit rate}}{2578}$ MHz, Jitter Tolerance*5 and Variable.
If the Variable option is selected, the following settings are available:
<table>
<tr><th>Bit Rate [Gbit/s]</th><th>Setting Range [MHz]</th><th>Step [MHz]</th></tr>
<tr><td>2.400000 to 5.500000</td><td>3</td><td>—</td></tr>
<tr><td>5.500001 to 7.500000</td><td>3 to 4</td><td>1</td></tr>
<tr><td>7.500001 to 9.500000</td><td>3 to 5</td><td>1</td></tr>
<tr><td>9.500001 to 10.500000</td><td>3 to 6</td><td>1</td></tr>
<tr><td>10.500001 to 12.500000</td><td>3 to 7</td><td>1</td></tr>
<tr><td>12.500001 to 14.500000</td><td>3 to 8</td><td>1</td></tr>
<tr><td>14.500001 to 15.500000</td><td>3 to 9</td><td>1</td></tr>
<tr><td>15.500001 to 17.500000</td><td>3 to 10</td><td>1</td></tr>
<tr><td>17.500001 to 19.500000</td><td>3 to 11</td><td>1</td></tr>
<tr><td>19.500001 to 20.500000</td><td>3 to 12</td><td>1</td></tr>
<tr><td>20.500001 to 22.500000</td><td>3 to 13</td><td>1</td></tr>
<tr><td>22.500001 to 24.500000</td><td>3 to 14</td><td>1</td></tr>
<tr><td>24.500001 to 25.500000</td><td>3 to 15</td><td>1</td></tr>
<tr><td>25.500001 to 27.500000</td><td>3 to 16</td><td>1</td></tr>
<tr><td>27.500001 to 29.500000</td><td>3 to 17</td><td>1</td></tr>
<tr><td>29.500001 to 30.500000</td><td>11 to 18</td><td>1</td></tr>
<tr><td>30.500001 to 32.100000</td><td>11 to 19</td><td>1</td></tr>
</table></td></tr>
<tr><td colspan="2">Jitter Tolerance</td></tr>
<tr><td>Clock Recovery</td><td>At the bit rate of 28.05 Gbit/s, conforming to Jitter Tolerance Mask defined by the “32G FC standard”
At the bit rate of 25.78125 Gbit/s, conforming to Jitter Tolerance Mask defined by the “100 GbE (25.78 × 4) standard”
At the bit rate of 14.0625 Gbit/s, conforming to Jitter Tolerance Mask defined by the “Infiniband FDR standard”
At the bit rate of 14.025 Gbit/s, conforming to Jitter Tolerance Mask defined by the “16G FC standard”
At the bit rate of 10.3125 Gbit/s, conforming to Jitter Tolerance Mask defined by the “10 GbE standard”</td></tr>
</table>

*1: The system clock can be selected only when option x22 is installed. Clock is recovered from the data input to the Data1 Input connector. The input pattern must be an NRZ PRBS pattern with a mark ratio of 1/2.
*2: When option x22 is installed.
*3: When option x01 is installed.
*4: When the option x22 is installed:
The target loop band is specified by the maximum setting value of each bit rate.
*5: The Jitter Tolerance option makes the loop band wider than the other options and enables the Jitter Tolerance measurement.

Jitter Tolerance

Jitter Tolerance	Bit rate: 16 Gbit/s, 28.1 Gbit/s*, 32.1 Gbit/s* Pattern: PRBS $2^{31} - 1$ SSC with a 5300 ppm amplitude and RJ of 0.3 UI can be simultaneously applied by using MU181500B. These specifications are defined assuming the following conditions: Loopback connection to the MU195020A, defined by one specific temperature in the range of 20° to 30°C. When RJ + BUJ is bigger than 0.5 UIp-p or SJ + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen.



Modulation Frequency [Hz]	Max. Modulation Amplitude [UIp-p]	Specification [UIp-p]
10	2,000	2,000
7,500	2,000	2,000
100,000	2,000	150
1,000,000	200	15
10,000,000	16	1
250,000,000	1	1

*: Option x01 available

Multichannel Operation

Combination*1	
Number of Channels	2
Pattern	At Combination n = 2 below (2ch combination)
Data	Pattern Length 2 × n to 268435456 × n bits, n bits step*2
Mixed	Row Length 2048 × n to (268435456 + 2^{31}) × n bits, 1024 × n bits step*2 Pattern Length 1024 × n to 268435456 × n bits, n bits step*2

*1: Combination extending over multiple slots cannot be set.
*2: Common to every channel specified by Combination Setting.

Automatic Measurement Function

Eye Contour	Measurement target Data 1 to Data n*1
Eye Margin	Measurement target Data 1 to Data n*1
Bathtub	Measurement target Data 1 to Data n*1
Capture	2Ch Combination is available*2
PAM4 BER Measurement	The following pattern selectable • GrayPRBS7, 9, 10, 11, 13Q-IEEE200G_400G [Draft2], 15,20 • GrayPrePRBS20 • GrayPreQPRBS13-CEI • GrayPreQPRBS13-IEEE100GBASE-KP4_Lane0, 1, 2, 3 • GrayPRQS10 • GrayQPRBS13-CEI • GrayQPRBS13-IEEE100GBASE-KP4_Lane0, 1, 2, 3 • GraySSPR • PRBS7, 9, 10, 11, 13Q-IEEE200G_400G [Draft2], 15, 20 • PrePRBS20 • PreQPRBS13-CEI • PRQS10 • QPRBS13-CEI • QPRBS13-IEEE100GBASE-KP4_Lane0, 1, 2, 3 • Squarewave • SSPR • SSPRQ • Transmitter_Linearity

*1: Separately specified for each channel.
*2: Common to every channel specified by Combination Setting.

Extension Function

PCIe	
Supported Standards	PCI Express Base Specification Revision4 .0 Version0 .5, 0 .7 Bit rate: PCIe Gen1/Gen2/Gen3/Gen4 Lane number: × 1 Test target: Root Complex, End Point
Required Option	MU195020A/40A-x10/x11/x22 or x20/x21/x22
Required Software	MX183000A-PL011: This software enables setting DUT to Loopback state by following PCIe LTSSM and generating a training sequence required for transition to Loopback state. MX183000A-PL021: This software enables setting DUT to Loopback state by following PCIe LTSSM and supporting negotiation with DUT. LTSSM state transition can be analyzed as log. (One MU195020A and one MU195040A are required for this software.) Adding MX183000A-PL001 to each option of the above software enables controlling MU195020A, MU181500B, MU195040A and supporting Jitter Tolerance Test.
Loopback Through	Configuration, Recovery
Test Pattern	Modified Compliance Pattern Insert Delay Symbol: Enable, Disable (Available for Gen1 and 2) Compliance Pattern Insert Delay Symbol: Enable, Disable (Available for Gen1 and 2) User PRSB
SRIS	Available when using MX183000A-PL021
SKP Ordered Set Insertion	Enable, Disable
SKP Length/Insertion	For Gen1, 2 Length: COM+1, COM+2, COM+3, COM+4, COM+5 Interval: 768 to 3076, 80 to 3076, 2 step For Gen3, 4 Length: 8, 12, 16, 20, 24 Interval: 187 to 750, 20 to 750, 1 step
Link Training Report	Available when using MX183000A-PL021
Counter	Tx SKP Count Rx SKP Count (when using MX183000A-PL021) Error Rate, Error Count (when using MX183000A-PL021)
LTSSM Log	Available when using MX183000A-PL021

General (MU195020A/MU195040A)

Dimensions and Mass	234 (W) × 21 (H) × 175 (D)mm (Excluding protrusions), 2.5 kg max.
Operating Temperature	15° to 35°C

Noise Generator MU195050A Specifications

Operating Bit Rate

Operating Bit Rate	2.4 Gbit/s to 32.1 Gbit/s

Data Input

Number of Channels	2
Number of Inputs per Channel	2 (Data, $\overline{\text{Data}}$) (Differential)
Input Amplitude	1.5 Vp-p max. (Single-end) 3.0 Vp-p max. (Differential)
Offset	–2.0 V to +3.3 V
Impedance	50Ω
Connector	K (f)

Data Output

The signal that is output from the noise source is AC-coupled.

Number of Channels	2
Number of Outputs per Channel	2 (Data, $\overline{\text{Data}}$) (Differential)
Insertion Loss	–3 dB +1/–2.5 dB*
Impedance	50Ω (Output Signal from noise source is AC-coupled)
Connector	K (f)

*: Defined for 12.890625 GHz and sine wave.

External Input

For connecting to USB3.1 Receiver Test Adapter G0373A or the Gating Output signal of MU195020A.

Number of Channels	1*
Number of Inputs Per Channel	2 (Differential)
Input Amplitude	1.5 Vp-p max. (Single-end) 3.0 Vp-p max. (Differential)
Impedance	50Ω, AC-coupled
Connector	SMA (f)

*: Data Input 1 Channel only

Differential Mode Interface (DMI)

The setting is common for Data Input 1 and Data Input 2. However, the Output Control can be turned On or Off individually.

Amplitude	4 mVp-p to 200 mVp-p (Differential)
Amplitude Setting Step	1 mV
Amplitude Accuracy	±20% ±10 mV*
Frequency	2 GHz to 10 GHz
Frequency Setting Step	10 MHz
Waveform	Sine wave
Presets	PCI Express Gen3, PCI Express Gen4
Output Control	Capability of switching On/Off of Data Input 1 Channel and Data Input 2 Channel simultaneously. (Either White Noise or External Input can be selected for Data Input 1 Channel). (Either Data Input 2 Channel or White Noise can be selected)

*: Defined at certain temperature between 20° to 30°C for 2.1 GHz, 4.2 GHz, 10 GHz.

Noise Generator MU195050A Specifications

Common Mode Interface (CMI)

The setting is common for Data Input 1 and Data Input 2. However, the Output Control can be turned On or Off individually.

Amplitude	10 mVp-p to 250 mVp-p (Single-end)
Amplitude Setting Step	2 mV
Amplitude Accuracy	±20% ±25 mV*
Frequency	Low Band: 100 MHz to 1 GHz High Band: 1 GHz to 6 GHz
Frequency Setting Step	Low Band: 1 MHz High Band: 10 MHz
Waveform	Sine wave
Presets	TBT3
Output Control	Capability of switching On/Off of Data Input 1 Channel and Data Input 2 Channel simultaneously. (Either DMI/CMI or External Input can be selected for Channel 1) (Either Channel 2 or DMI/CMI can be selected)

*: Defined at certain temperature between 20° to 30°C for 120 MHz, 400 MHz, 1 GHz, 6 GHz.

White Noise

The setting is common for Data Input 1 and Data Input 2.

Flatness	±5 dB (10 MHz to 10 GHz)
Crest Factor	>5 (p-p/rms)
Amplitude	0.2 mV rms to 25 mV rms
Amplitude Setting Step	0.2 mV rms
Amplitude Accuracy	±20% ±2.5 mVrms*
On/Off	Capability of switching On/Off of Data Input 1 Channel and Data Input 2 Channel simultaneously. (Either DMI/CMI or External Input can be selected for Channel 1) (Either Channel 2 or DMI/CMI can be selected)

*: Defined at one specific temperature between 20 to 30°C, subtracting the residual noise value from the data by sampling oscilloscope with 50 GHz bandwidth.

General

Dimensions and Mass	234 (W) × 21 (H) × 175 (D) mm (Excluding protrusions) 1.2 kg max.
Operating Temperature	+15° to +35°C
Storage Temperature	–20° to +60°C

Refer to the MP1800A brochure for the 12.5 GHz 4 Port Synthesizer MU181000B and Jitter Modulation Source MU181500B.

Note:

Note:

Anritsu envision : ensure

Specifications are subject to change without notice.

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